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DATA SHEET

AT070TNA2 V.1

ROHS

ISSUE	VERSION	APPROVER	CHECKER	ENGINEER
2010/09/13	C	批准 2011.07.19 利聚盛	KENNY	ALLEN

CHIMEI INNOLUX DISPLAY CORPORATION

LCD MODULE

APPLICATION NOTE

Customer: _____
LCD SIZE: 7.0SD
Date: 2010/9/13
Version: C

Remark
■Without PCB

Approved by	Reviewed by	Prepared by
Hans Chen 2010/9/15	David Tang 2010/9/15	YC Guan 2010/9/13

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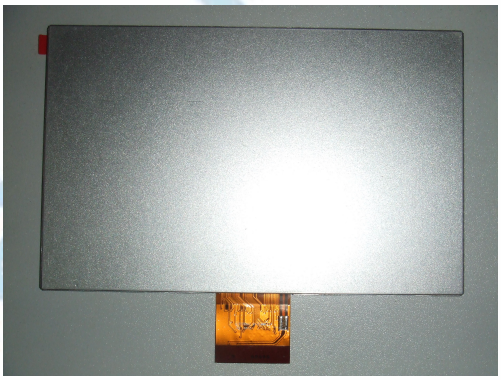
Record of Revision

Version	Revise Date	Page	Content
A	2010-02-26		Initial Release
B	2010-7-28	11	Adding TTL to LVDS reference circuit
C	2010-9-13		Adding model AT070TNA2 V.1

1. Module Introduction

1.1 Module Photo

Model	Module photo	
	Top side	Bottom side
AT070TNA2 V.1		
AT070TNA2		

1.2 Module Comparison Table

Module name	Brightness(nits)	Pin Num.	Recommended connector
AT070TNA2 V.1	250	40	FH12A-40S-0.5SH
AT070TNA2	250	40	I-PEX 20455-040E-02

2. Pin Assignment Table

Pin No.	Symbol		I/O	Function	
	AT070TNA2	AT070TNA2 V.1			Remark
1	VCOM	VCOM	P	Common Voltage	
2	VDD	VDD	P	Power Voltage for digital circuit	
3	VDD	VDD	P	Power Voltage for digital circuit	

4	NC	NC	---	No connection	
5	Reset	Reset	I	Global reset pin	
6	STBYB	STBYB	I	Standby mode, Normally pulled high STBYB = “1”, normal operation STBYB = “0”, timing controller, source driver will turn off, all output are High-Z	
7	GND	GND	P	Ground	
8	RXIN0-	RXIN0-	I	- LVDS differential data input	
9	RXIN0+	RXIN0+	I	+ LVDS differential data input	
10	GND	GND	P	Ground	
11	RXIN1-	RXIN1-	I	- LVDS differential data input	
12	RXIN1+	RXIN1+	I	+ LVDS differential data input	
13	GND	GND	P	Ground	
14	RXIN2-	RXIN2-	I	- LVDS differential data input	
15	RXIN2+	RXIN2+	I	+ LVDS differential data input	
16	GND	GND	P	Ground	
17	RXCLKIN-	RXCLKIN-	I	- LVDS differential clock input	
18	RXCLKIN+	RXCLKIN+	I	+ LVDS differential clock input	
19	GND	GND	P	Ground	
20	RXIN3-	RXIN3-	I	- LVDS differential data input	
21	RXIN3+	RXIN3+	I	+ LVDS differential data input	
22	GND	GND	P	Ground	
23	NC	NC	---	No connection	
24	NC	NC	---	No connection	
25	GND	GND	P	Ground	
26	NC	NC	---	No connection	
27	NC	DIMO	---	Backlight CABC controller signal output	
28	SELB	SELB	I	6bit/8bit mode select	
29	AVDD	AVDD	P	Power for Analog Circuit	
30	GND	GND	P	Ground	
31	LED-	LED-	P	LED Cathode	

32	LED-	LED-	P	LED Cathode	
33	LED-	L/R	P	LED Cathode	
34	VGL	U/D	P	Gate OFF Voltage	
35	NC	VGL	---	No connection	
36	NC	CABCEN1	I	CABC Enable	
37	VGH	CABCEN0	I/P	CABC Enable	
38	LED+	VGH	P	Gate ON voltage	
39	LED+	LED+	P	LED Anode	
40	LED+	LED+	P	LED Anode	

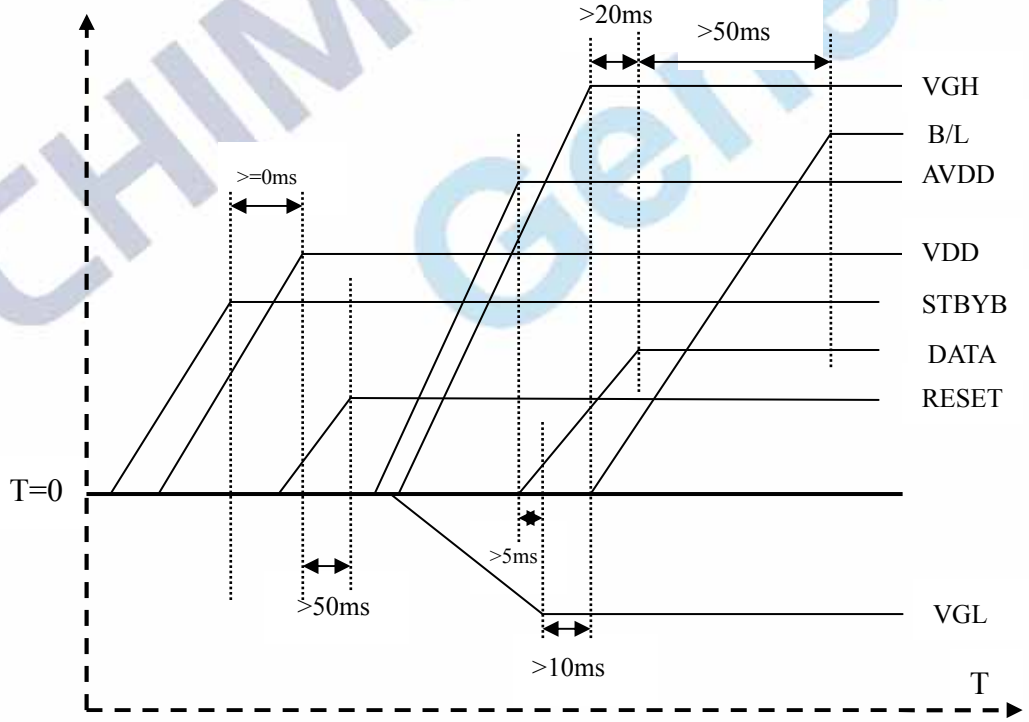
Note: I: input, O: output, P: Power

3. Power &Timing Characteristic

3.1. Power Sequence

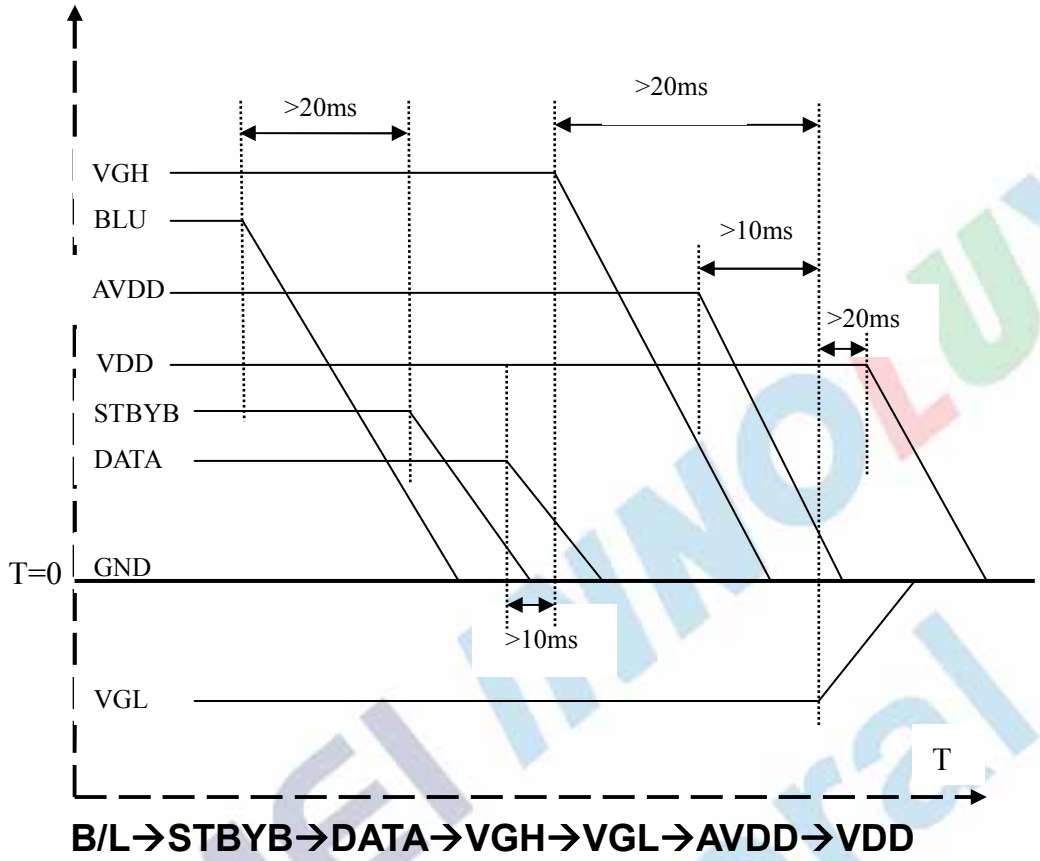
Customer should follow our product power sequence, other it would lead to display abnormal, please refer to the figures as below.

Power on:



STBYB→VDD→AVDD→VGL→VGH→DATA→B/L

Power off:



3.2 Power Operation Conditions

Customer should notice the red mark specially, if you do not follow it, it would lead to display abnormal.

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power voltage	DV_{DD}	3.0	3.3	3.6	V	Note 2
	AV_{DD}	10.8	11	11.2	V	
	V_{GH}	19.7	20	20.3	V	
	V_{GL}	-6.5	-6.8	-7.1	V	
Input signal voltage	V_{COM}	2.8	(3.8)	4.8	V	
Input logic high voltage	V_{IH}	0.7 DV_{DD}	-	DV_{DD}	V	Note 3
Input logic low voltage	V_{IL}	0	-	0.3 DV_{DD}	V	

Note 1: Be sure to apply DV_{DD} and V_{GL} to the LCD first, and then apply V_{GH}.

Note 2: DV_{DD} setting should match the signals output voltage (refer to Note 3) of customer's system board.

Note 3:RESET,STBYB.

3.3 Timing Description

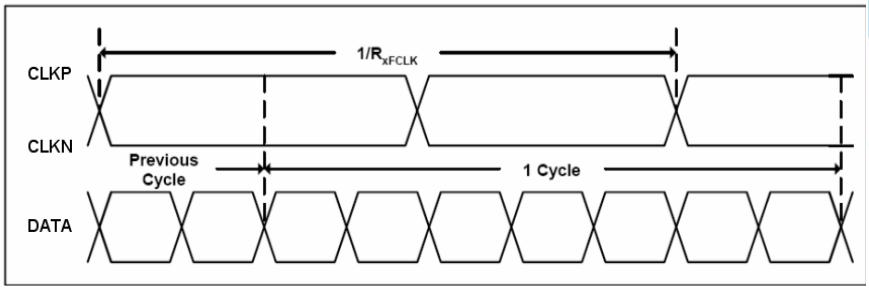
Input signals must follow our timing specification, Otherwise the LCM will display abnormally.

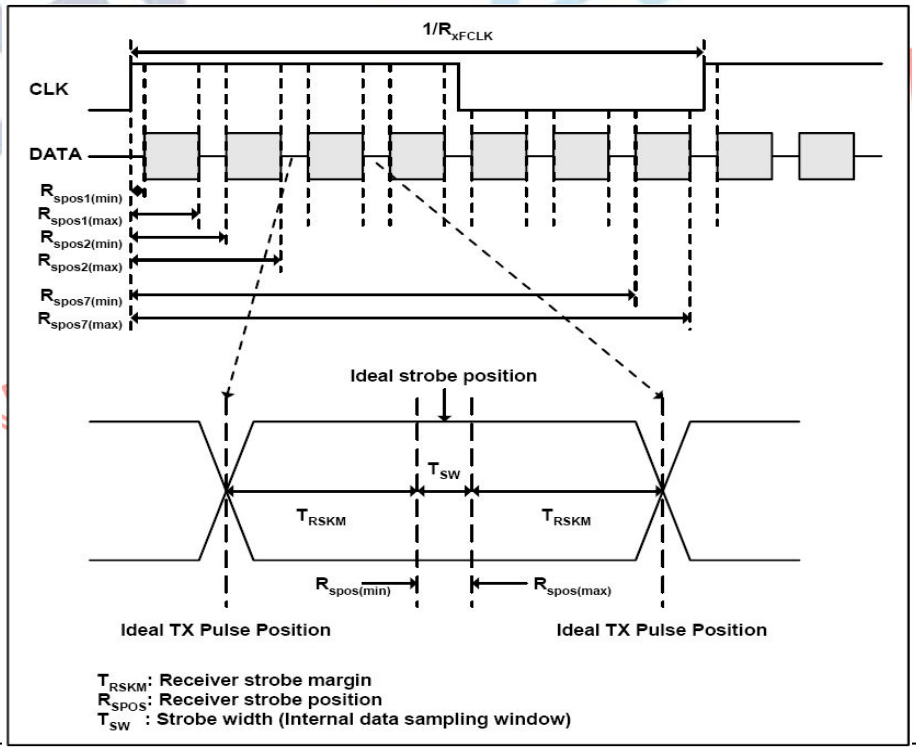
About the detail timing parameters of LCD display, please follow the product specification.

3.3.1AC Electrical Characteristics

Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock frequency	R_{xFCLK}	40.8	51.2	71	MHz	
Input data skew margin	T_{RSKM}	500	-	-	ps	
Clock high time	T_{LVCH}	-	$4/(7* R_{xFCLK})$	-	ns	
Clock low time	T_{LVCL}	-	$3/(7* R_{xFCLK})$	-	ns	

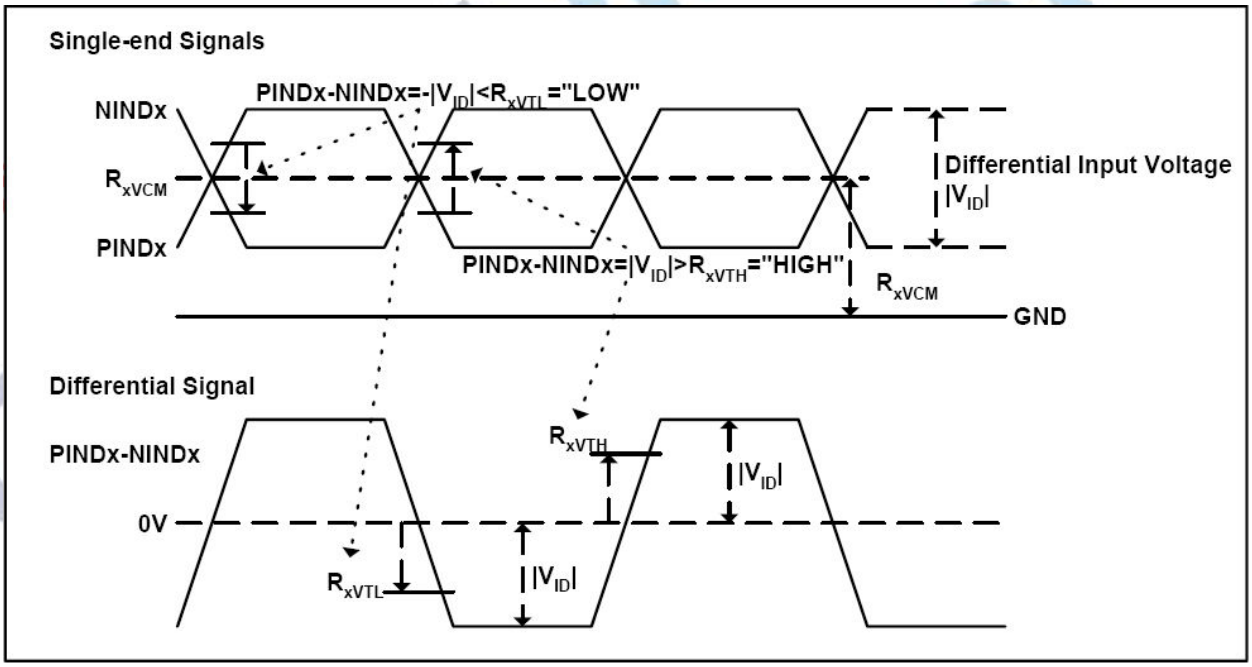
3.3.2 Input Clock and Data Timing Diagram





3.3.3 DC Electrical Characteristics

Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Differential input high Threshold voltage	R_{xVTH}	-	-	+0.1	V	R_{XVCM}=1.2V
Differential input low Threshold voltage	R_{xVTH}	-0.1	-	-	V	
Input voltage range (singled-end)	R_{xVIN}	0	-	2.4	V	
Differential input common mode voltage	R_{xVCM}	$\|V_{ID}\|/2$	-	$2.4-\|V_{ID}\|/2$	V	
Differential voltage	$\|V_{ID}\|$	0.2	-	0.6	V	
Differential input leakage current	RV_{xliz}	-10	-	+10	uA	



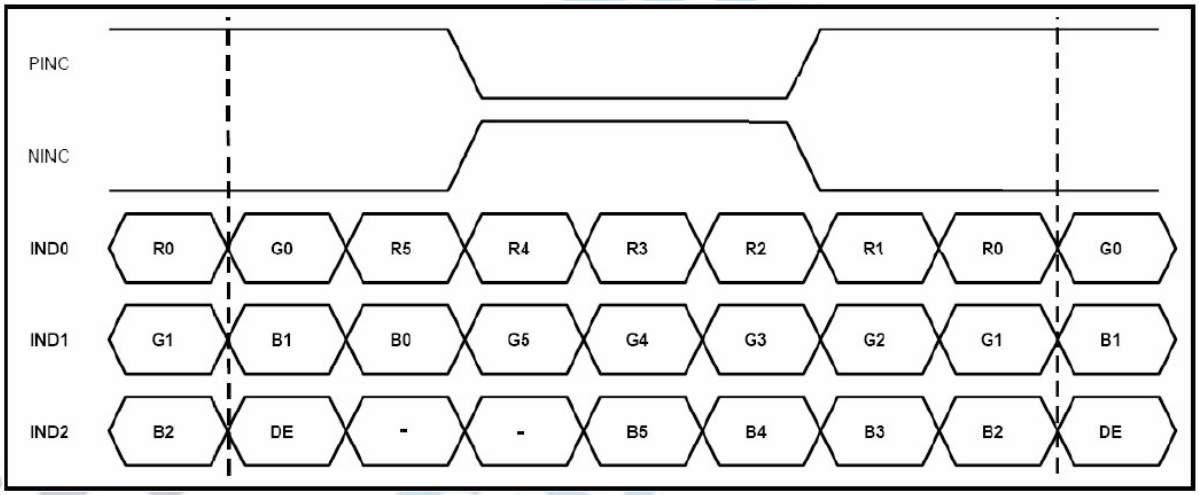
2.3.4 Timing

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Clock Frequency	fclk	40.8	51.2	67.2	MHz	Frame rate =60Hz

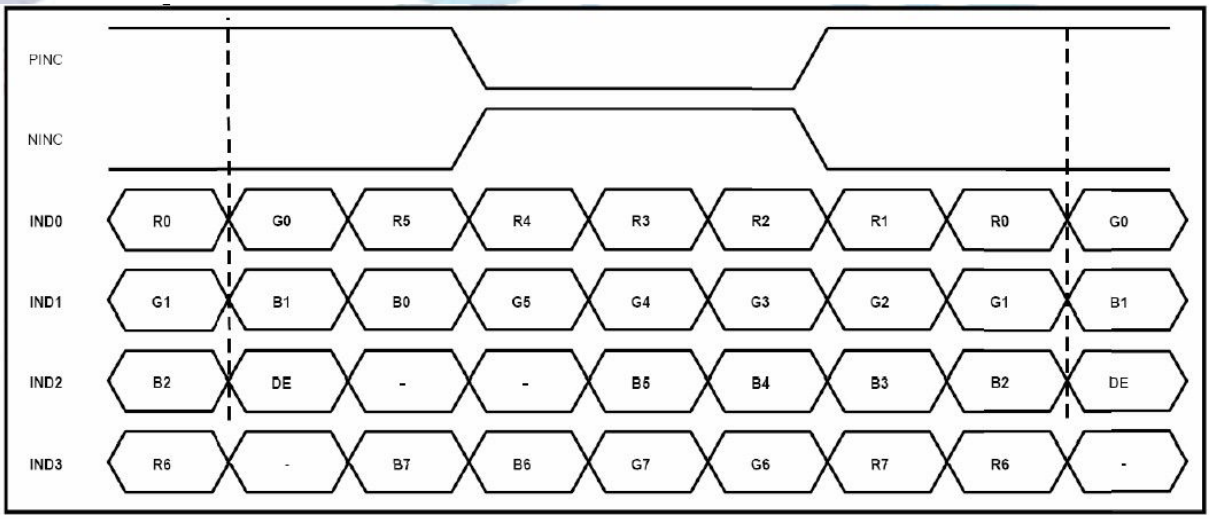
Horizontal display area	thd	1024			DCLK	
HS period time	th	1114	1344	1400	DCLK	
HS Blanking	thb	90	320	376	DCLK	
Vertical display area	tvd	600			H	
VS period time	tv	610	635	800	H	
VS Blanking	thb	10	35	200	H	

2.3.5 Data Input Format

6bit LVDS input



8bit LVDS input



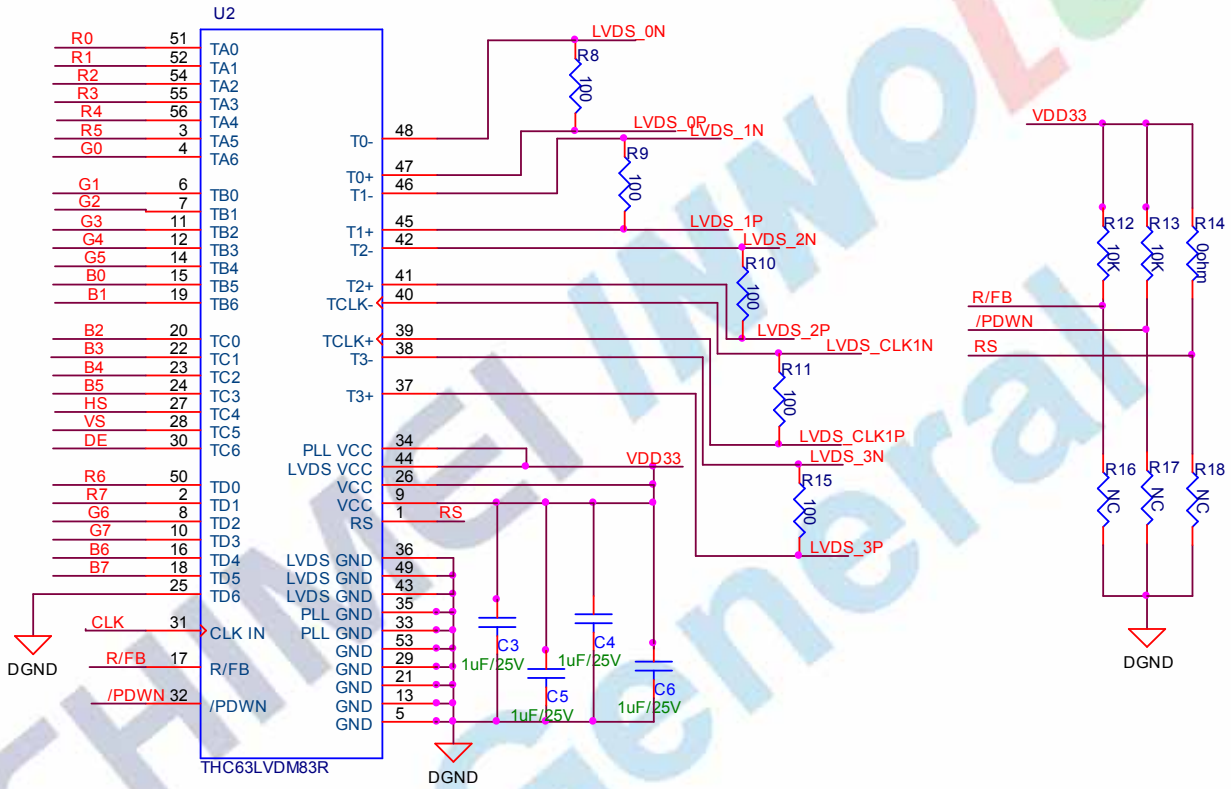
Remark: Support DE mode only, SYNC mode is not supported.

4. Software Introduction

NA

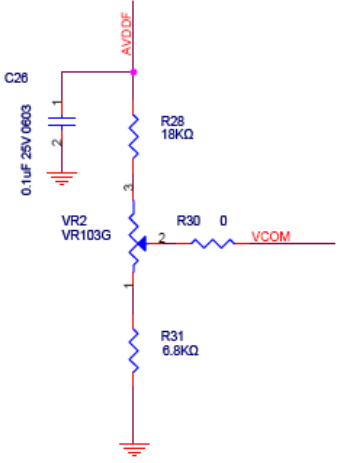
5. Reference Circuit

5.1 TTL to LVDS reference circuit

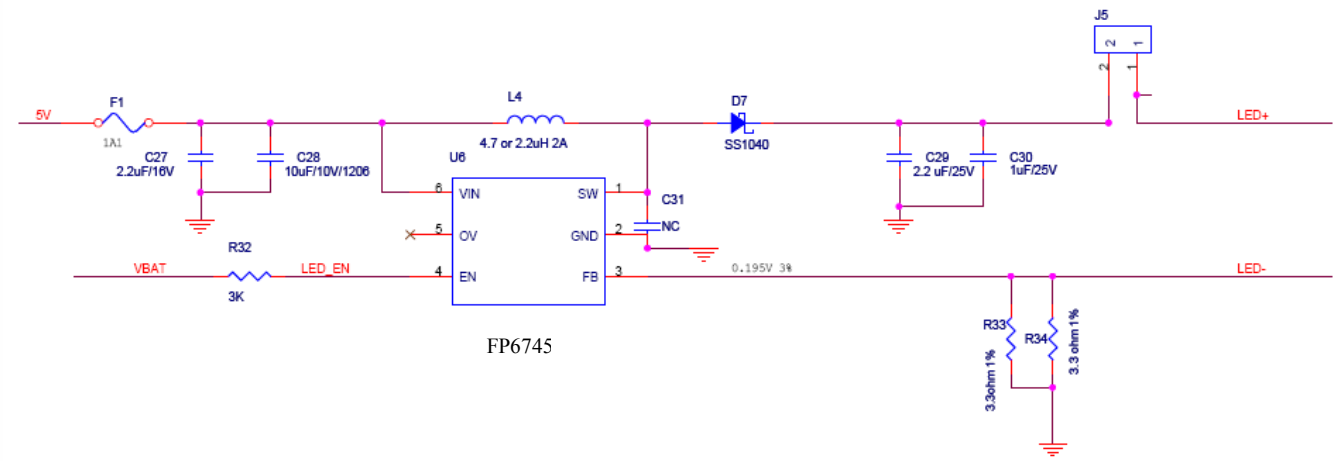


Remark: If the data output is TTL interface, this reference circuit can be used to adapt the LVDS interfacef for this LCM.

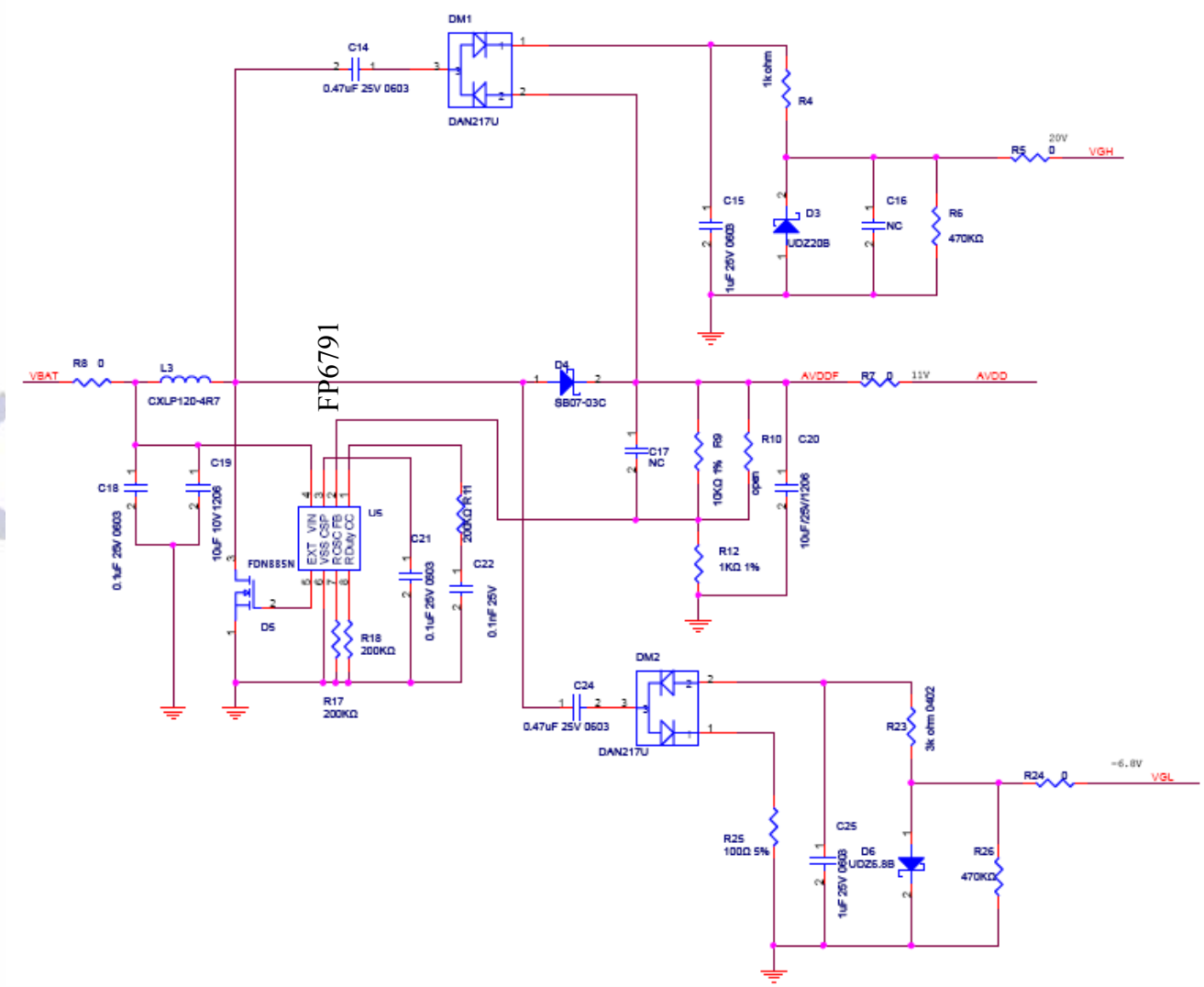
5.2 Vcom Reference Circuit



5.3 Backlight Driver Reference Circuit



5.4 DC/DC Reference Circuit



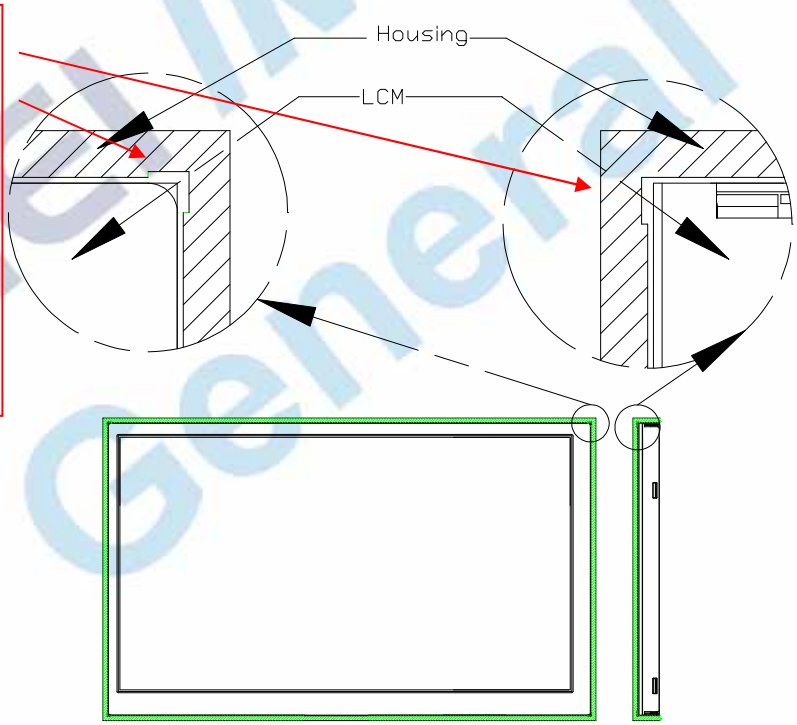
5.5 Vendor Recommend

Item	Vendor	Type	Remark
DC/DC	Fiti Power	FP6791	
LED Driver	Fiti Power	FP6745	PWM Frequency:100Hz~50KHz

6.Suggestions for housing design.

6.1 LCM corner /edge avoidable cutting.

If you design a avoidable cutting as the right drawing. LCM will easier to assemble in the housing.
When you use the LCM with TSP, the cutting will avoid damage the edge or corner of TSP during the assembly.



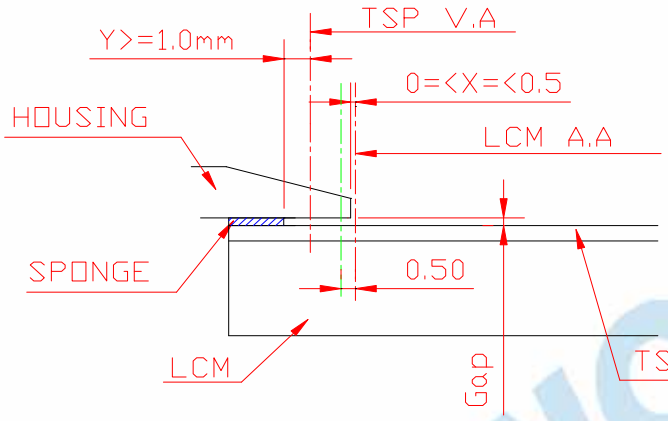
Suggestions of housing design

6.2 Housing opening design guide.

6.2.1 With TSP

Because touch film is made of flexible PET, any unexpected touch with it would cause malfunction of touch panel. So here a sponge between touch panel and plastic housing is

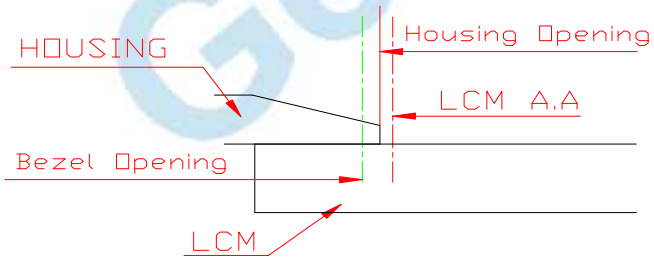
recommended for users. And the drawing will show you how to design the housing and sponge.



Section sketch (with TSP)

Notes: 1. X is the distance from LCM A.A to housing opening.
2. Y is the distance from TSP V.A to Sponge opening.
3. The active force will be bigger when you touch the area near the housing opening.
4. If you want to provide more protection for LCM, you can add same buffer material on the bottom of LCM.

6.2.2 Without TSP



Section sketch(without TSP)

Notes: 1. Housing opening mast bigger than LCMA.A and cover the bezel .
2. If you want to provide more protection for LCM, you can add same buffer material on the top or bottom of LCM.